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(54) **THIN FILM TRANSISTOR AND ORGANIC ELECTROLUMINESCENCE DISPLAY USING THE SAME**

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(57) **ABSTRACT**

A thin film transistor (TFT) having a lightly doped drain (LDD) structure includes a lightly doped drain (LDD) region formation pattern, an active layer formed in an uneven structure on the LDD region formation pattern, and having a source region and a drain region having an LDD region. A gate electrode may be formed on a gate insulating layer, and source and drain electrodes are coupled to the source and drain regions.

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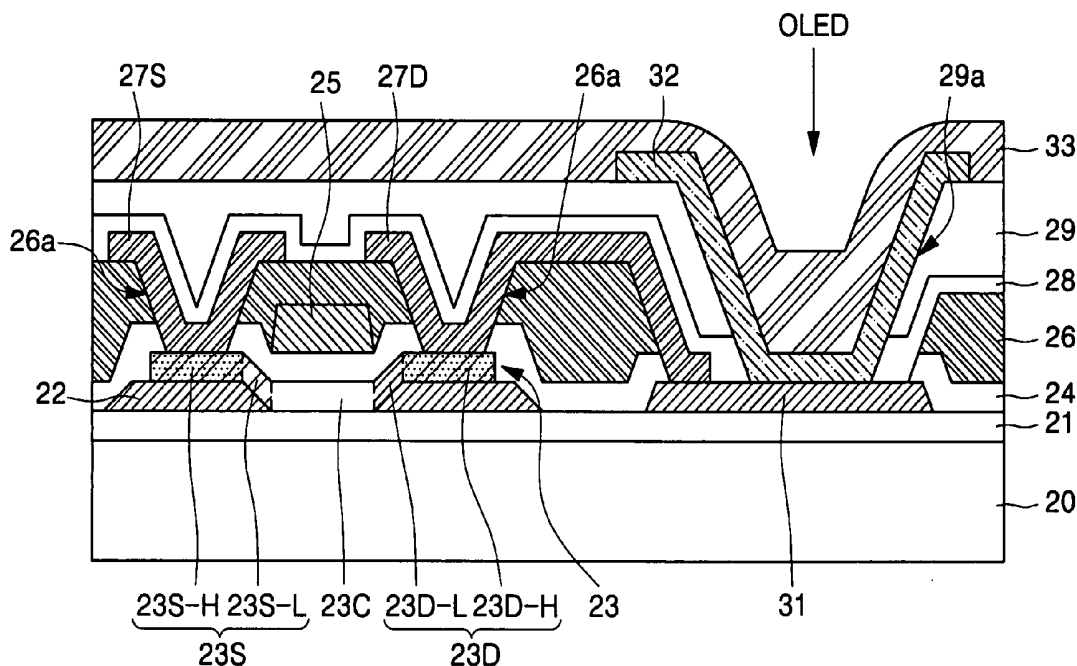


FIG. 1A  
(PRIOR ART)

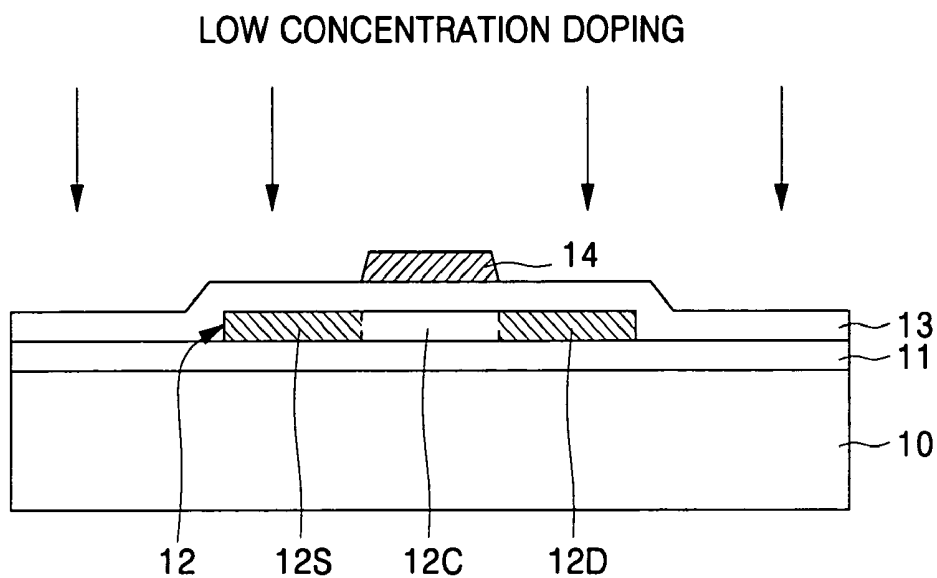


FIG. 1B  
(PRIOR ART)

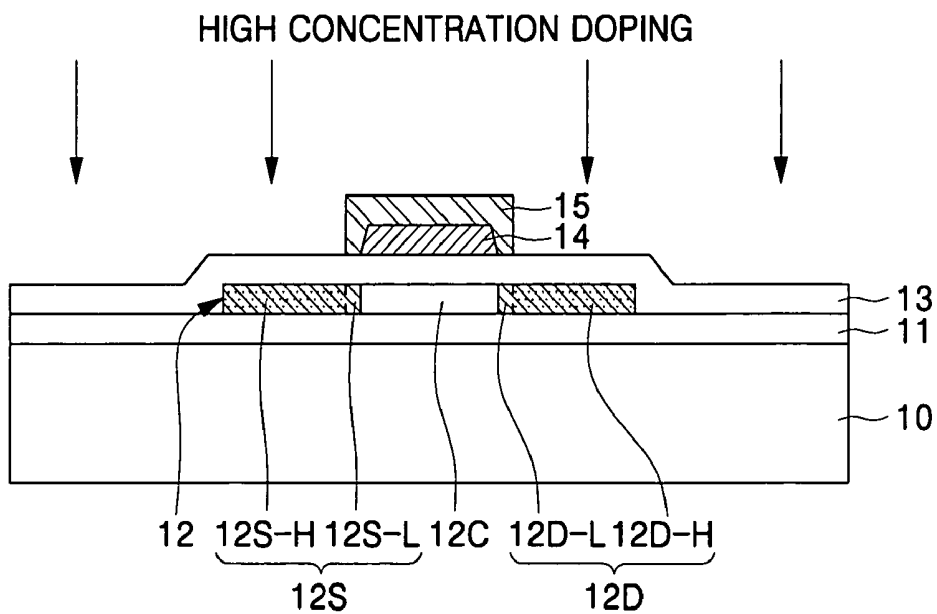


FIG. 1C  
(PRIOR ART)

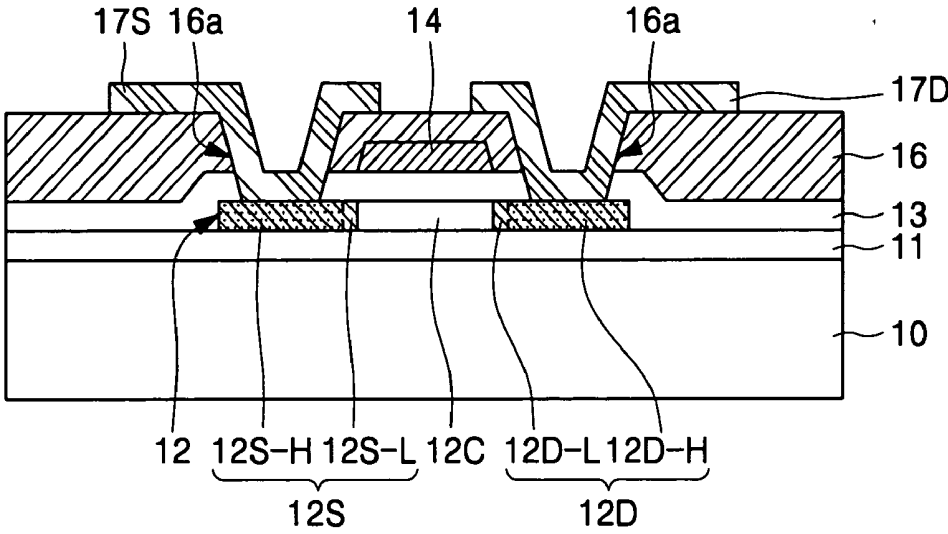


FIG. 2A

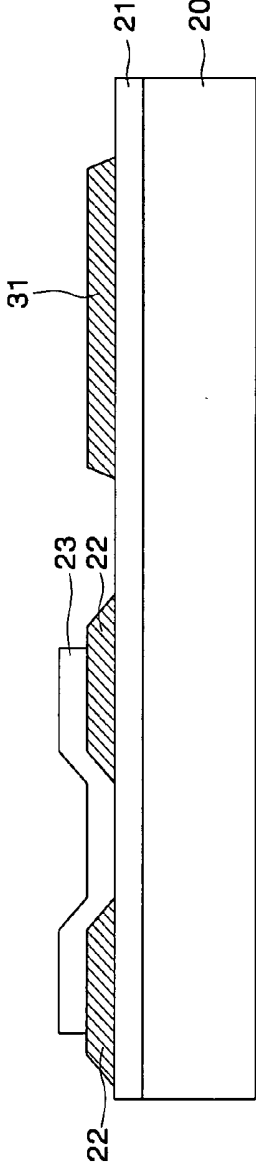


FIG. 2B

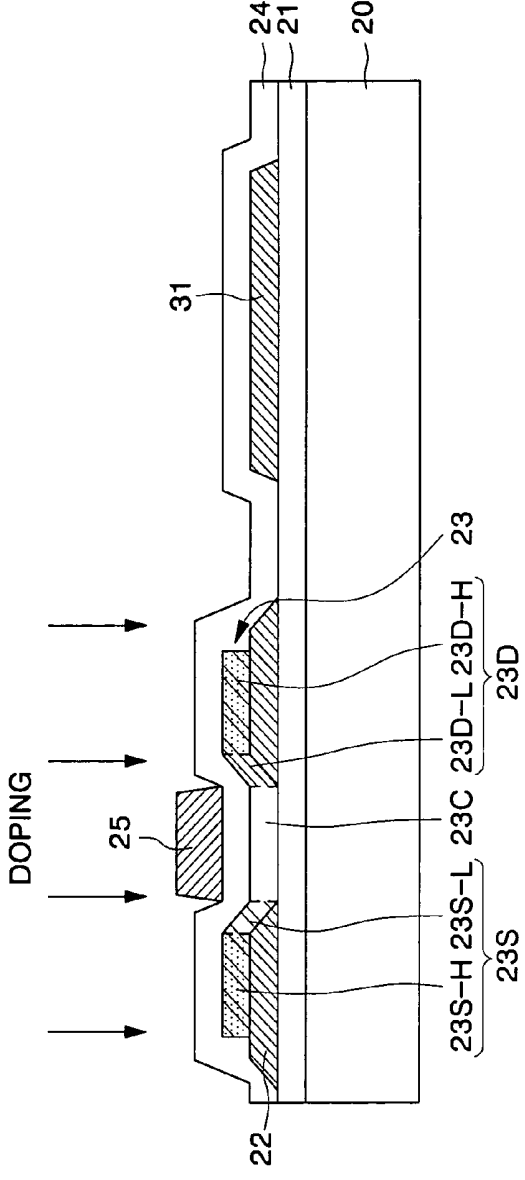


FIG. 2C

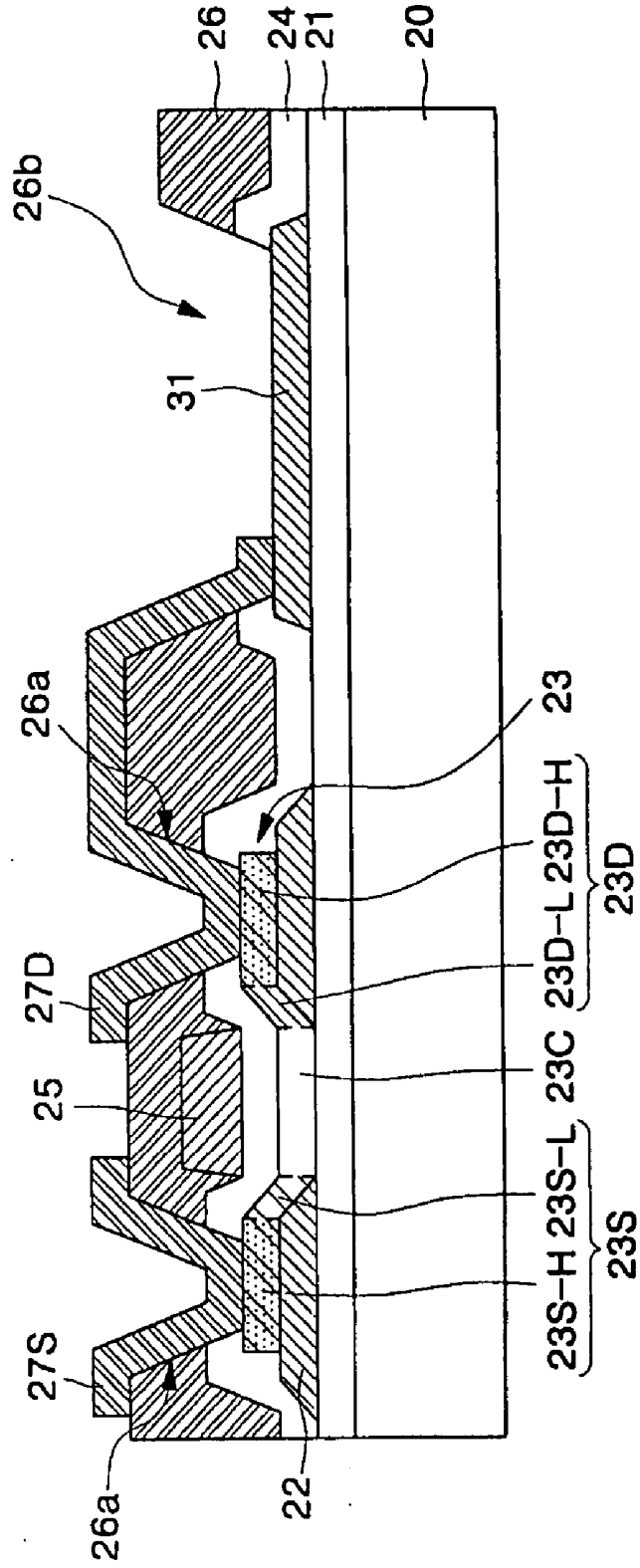


FIG. 2D

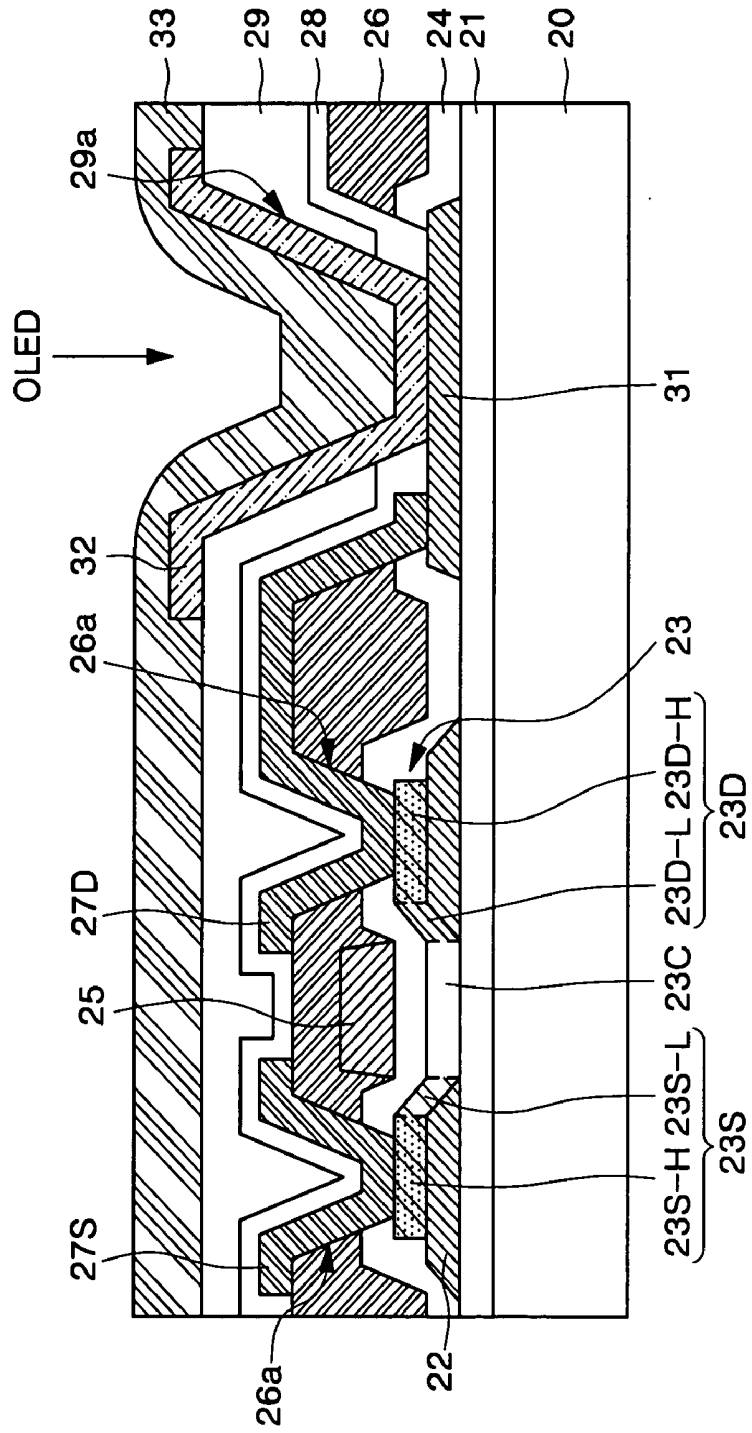


FIG. 3A

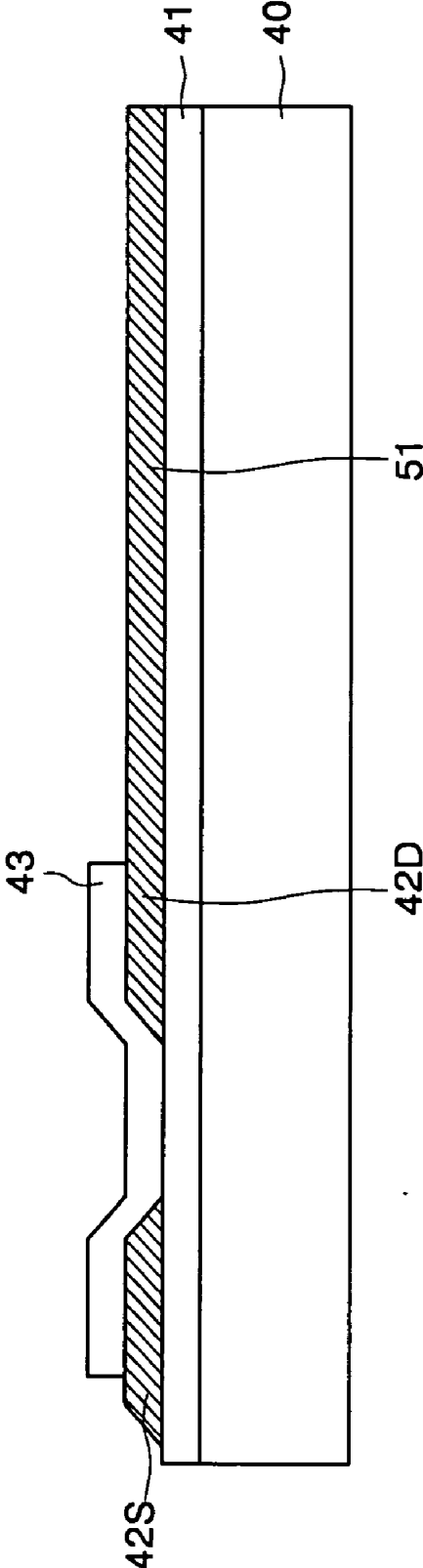


FIG. 3B

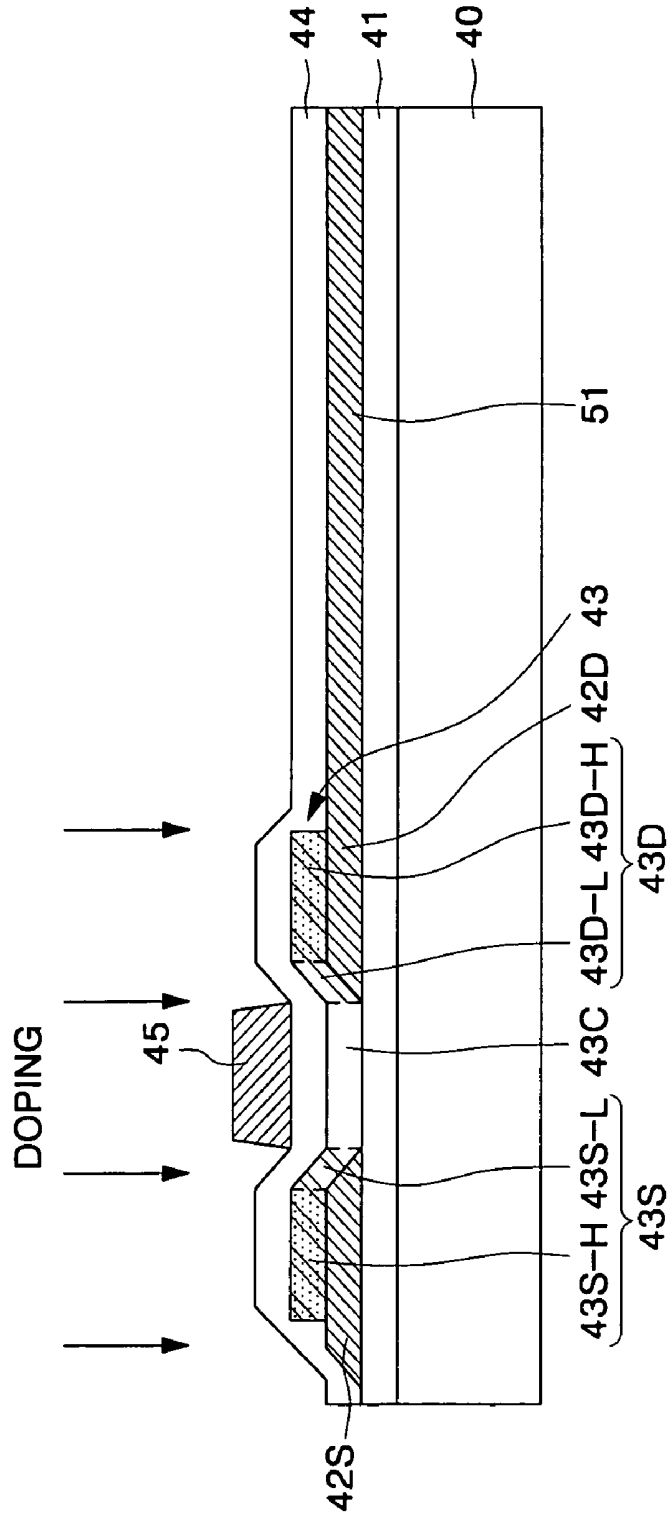
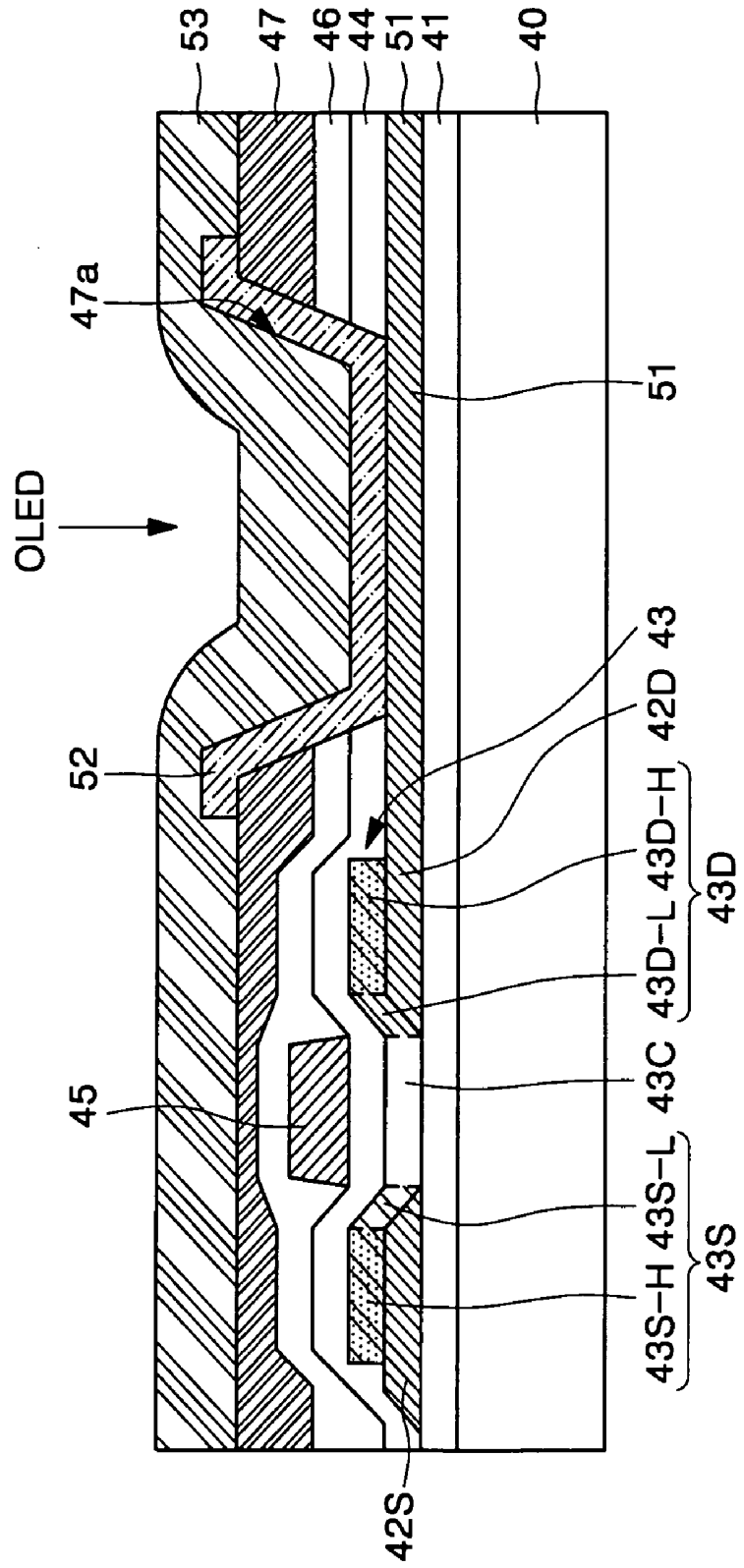


FIG. 3C



**THIN FILM TRANSISTOR AND ORGANIC  
ELECTROLUMINESCENCE DISPLAY USING THE  
SAME**

**CROSS-REFERENCE TO RELATED  
APPLICATION**

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2004-0029508, filed Apr. 28, 2004, which is hereby incorporated by reference for all purposes as if fully set forth herein.

**BACKGROUND OF THE INVENTION**

[0002] 1. Field of the Invention

[0003] The present invention relates to a thin film transistor (TFT) and an electroluminescence display using the same and, more particularly, to a TFT having a lightly doped drain (LDD) structure and an organic electroluminescence display using the same.

[0004] 2. Discussion of the Background

[0005] Generally, in an active matrix organic electroluminescence display that uses a TFT as a switching device, a pixel driving TFT may be formed in each pixel to drive the pixel, and a TFT may be used in a driving circuit that drives the pixel driving TFT and applies a signal to a scan line (i.e., gate line) and a signal line (i.e., data line).

[0006] A polycrystalline silicon TFT may be fabricated at a temperature similar to an amorphous silicon TFT, and it may have higher electron or hole mobility compared to the amorphous silicon TFT. Additionally, it may be possible to implement a complementary metal-oxide semiconductor (CMOS) TFT having an n-channel and a p-channel so that the driving circuit TFT and the pixel driving TFT may be simultaneously formed on a large-sized insulating substrate.

[0007] However, in an NMOS TFT of the CMOS polycrystalline silicon TFT, phosphorus (P) is typically used as a doping ion, and because phosphorus has mass relatively larger than that of boron (B), which is typically used for fabricating a PMOS TFT, silicon crystal may be destroyed, resulting in a damaged region. The damaged region may not be fully recovered even in subsequent activation processes.

[0008] This damaged region may cause hot carrier stress, in which electrons may penetrate a gate insulating layer or a MOS interface when they accelerate from a source region to a drain region. Furthermore, the hot carrier stress may reduce electron mobility, which adversely affects stability of circuit operation in the organic electroluminescence display, and may increase an off current.

[0009] In order to solve this problem, a method for forming a lightly doped drain (LDD) and a LDD structure has been suggested in which certain portions of source and drain regions are doped at a low concentration to reduce an off-current and minimize a reduction in on current.

[0010] FIG. 1A, FIG. 1B and FIG. 1C are cross-sectional views showing a TFT with a conventional LDD structure.

[0011] Referring to FIG. 1A, a polycrystalline silicon (poly-Si) layer may be formed by depositing and crystallizing amorphous silicon on an insulating substrate 10 having a buffer layer 11 using plasma enhanced chemical vapor

deposition (PECVD), low pressure chemical vapor deposition (LPCVD), sputtering, or other like methods.

[0012] After forming the poly-Si layer, photoresist may then be formed on it to form an active layer, and an active layer 12 may be formed by patterning the poly-Si layer using the photoresist as a mask.

[0013] A gate insulating layer 13 may then be deposited on the active layer 12, and a gate metal may be deposited on the gate insulating layer 13. A gate electrode 14 may then be formed by patterning the gate metal.

[0014] After forming the gate electrode 14, low concentration doping may be carried out using the gate electrode 14 as a mask to form an LDD region in the active layer, thus defining source and drain regions 12S and 12D. A region between the source and drain regions 12S and 12D acts as a channel region 12C of the TFT.

[0015] Referring to FIG. 1B, after forming the source and drain regions 12S and 12D, a photoresist pattern 15, for forming the source and drain regions 12S and 12D having the LDD region of the TFT, may be formed by applying and exposing photoresist on the insulating substrate 10.

[0016] After forming the photoresist pattern 15, LDD regions 12S-L and 12D-L and highly doped regions 12S-H and 12D-H may be formed by performing high concentration doping into the active layer using the photoresist pattern 15 as a mask.

[0017] Referring to FIG. 1C, after the high concentration doping, contact holes 16a, which expose a portion of the source and drain regions 12S and 12D, may be formed by forming and patterning an interlayer insulating layer 16 on an entire surface of the insulating substrate 10 having the gate electrode 14.

[0018] Next, a conductive layer may be deposited on the entire surface of the insulating substrate 10 and be subjected to photolithography to form source and drain electrodes 17S and 17D, which are electrically connected to the source and drain regions 12S and 12D via the contact holes 16a, thereby forming the TFT.

[0019] However, forming the TFT as described above requires a separate mask process to form the LDD region, which increases manufacturing time and cost.

**SUMMARY OF THE INVENTION**

[0020] The present invention provides a TFT having an LDD structure, and an organic electroluminescence display using the same, that may be formed without using a separate mask.

[0021] Additional features of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention.

[0022] The present invention discloses a TFT comprising a lightly doped drain (LDD) region formation pattern and an active layer formed in an uneven structure on the LDD region formation pattern, and having a source region and a drain region including an LDD region

[0023] The present invention also discloses a display comprising a lightly doped drain (LDD) region formation

pattern and a pixel electrode formed on a same layer on an insulating substrate, an active layer formed in an uneven structure on the LDD region formation pattern, and having a source region and a drain region including an LDD region, a gate electrode formed on a gate insulating layer, and a source electrode and a drain electrode coupled to the source and drain regions, respectively. Either the source electrode or the drain electrode is coupled to the pixel electrode.

[0024] The present invention also discloses a TFT comprising a source electrode and a drain electrode formed on an insulating substrate, and an active layer formed in an uneven structure on the source electrode and the drain electrodes and having a source region and a drain region including an LDD region.

[0025] The present invention also discloses a display comprising a source electrode, a drain electrode, and a pixel electrode formed on a same layer on an insulating substrate, and an active layer having a source region and a drain region including an LDD region, and formed in an uneven structure on the source and drain electrodes. A gate insulating layer is formed on an entire surface of the insulating substrate having the active layer, and a gate electrode is formed on the gate insulating layer. An insulating layer is formed on an entire surface of the insulating substrate having the gate electrode, and it has an opening that defines an emission region by exposing a portion of the pixel electrode. An organic layer is formed on the opening of the insulating layer, and an upper electrode is formed on an entire surface of the insulating substrate.

[0026] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0028] FIG. 1A, FIG. 1B and FIG. 1C are cross-sectional views showing a manufacturing process of a TFT having a conventional LDD structure.

[0029] FIG. 2A, FIG. 2B, FIG. 2C and FIG. 2D are cross-sectional views showing a manufacturing process of an organic electroluminescence display according to a first exemplary embodiment of the present invention.

[0030] FIG. 3A, FIG. 3B and FIG. 3C are cross-sectional views showing a manufacturing process of an organic electroluminescence display according to a second exemplary embodiment of the present invention.

#### DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0031] Hereinafter, exemplary embodiments of the present invention will be described with reference to the accompanying drawings.

[0032] FIG. 2A, FIG. 2B, FIG. 2C and FIG. 2D are cross-sectional views showing a manufacturing process of

an organic electroluminescence display according to a first exemplary embodiment of the present invention.

[0033] Referring to FIG. 2A, a buffer layer 21 (or, diffusion barrier) may be deposited on an insulating substrate 20 by PECVD, LPCVD, sputtering, or other like methods. The buffer layer 21 may prevent insulating substrate impurities, such as metal ions, from diffusing and penetrating a poly-Si active layer.

[0034] While a glass or plastic substrate may be used as the insulating substrate 20, glass is preferable.

[0035] After forming the buffer layer 21, a pixel electrode 31 and an LDD region formation pattern 22 may be formed on the buffer layer 21 by depositing and patterning a transparent conductive material, such as ITO, IZO or other like materials.

[0036] Edge portions of the pixel electrode 31 and the LDD region formation pattern 22 may have a taper angle of about 10° to about 45°.

[0037] Next, an amorphous silicon layer may be deposited on an entire surface of the insulating substrate by PECVD, LPCVD, sputtering, or other like methods. The amorphous silicon layer may be unevenly formed along the shape of the LDD region formation pattern 22 because the amorphous silicon layer on the edge portion of the LDD region formation pattern 22 may be formed along the edge portion's taper angle.

[0038] A dehydrogenation process may be carried out in a vacuum furnace after forming the amorphous silicon layer. The dehydrogenation process may not be carried out when the amorphous silicon layer is deposited by the LPCVD or sputtering method.

[0039] A poly-Si layer may be formed by crystallizing the amorphous silicon layer through an amorphous silicon crystallization process in which high energy is irradiated to the amorphous silicon layer. A crystallization process using a laser, such as excimer laser annealing (ELA), sequential lateral solidification (SLS) or other like processes, may be employed as the crystallization process.

[0040] After crystallization, a portion of the poly-Si layer on the edge portion of the LDD region formation pattern 22 may have a lower crystallinity than a portion of the poly-Si layer on the other portion of the LDD region formation pattern 22.

[0041] This is because the portion of the amorphous silicon layer on the edge portion of the LDD region formation pattern 22 may be thicker than the portion of the amorphous silicon layer on the other portion of the LDD region formation pattern 22.

[0042] After forming the poly-Si layer, photoresist may be formed on the poly-Si layer. Patterning the poly-Si layer using the photoresist as a mask forms an active layer 23.

[0043] The active layer 23 may be uneven due to the below LDD region formation pattern 22. A portion of the active layer 23 on the edge portion of the LDD region formation pattern 22 may be formed in a shape inclined by 10° to 45° according to the taper angle of the edge portion of the LDD region formation pattern 22.

[0044] Referring to FIG. 2B, after forming the active layer 23, a gate electrode 25 may be formed by depositing a gate insulating layer 24 on the active layer 23, depositing a gate metal on the gate insulating layer 24, and then patterning the gate metal.

[0045] Next, source and drain regions 23S and 23D may be formed by doping impurity ions at a high concentration into the active layer 23 using the gate electrode 25 as a mask. A region between the source and drain regions 23S and 23D acts as the TFT's channel region 23C.

[0046] An inclined portion of the source and drain regions 23S and 23D on the edge portion of the LDD region formation pattern 22 may act as a region having a lower doping concentration, namely, LDD regions 23S-L and 23D-L, as compared to other portions 23S-H and 23D-H of the source and drain regions 23S and 23D on the other portions of the LDD region formation pattern 22. Portions of the source and drain regions 23S and 23D on the other portions of the LDD region formation pattern 22 may act as highly doped regions 23S-H and 23D-H.

[0047] This is because the inclined portion of the active layer 23 on the edge portion of the LDD region formation pattern 22 may have less crystallinity than the non-inclined portions of the active layer 23 formed on other portions of the LDD region formation pattern 22, resulting in a lower doping degree of impurity.

[0048] Referring to FIG. 2C, after forming the source and drain regions 23S and 23D with the LDD regions 23S-L and 23D-L, an interlayer insulating layer 26 may be formed on the entire surface of the insulating substrate 10 having the gate electrode 25.

[0049] An activation process may then be performed in which doped impurities in the active layer 23 are further activated through annealing in a furnace.

[0050] After performing the annealing process, contact holes 26a, which expose a portion of the source and drain regions 23S and 23D, may be formed by patterning the interlayer insulating layer 26, while simultaneously forming an opening 26b exposing the pixel electrode 31.

[0051] Next, source and drain electrodes 27S and 27D, which are coupled to the source and drain regions 23S and 23D via the contact holes 26a, may be formed by depositing and patterning a conductive layer on the entire surface of the insulating substrate 20, thus forming the TFT.

[0052] Further, either the source electrode or the drain electrode 27S, 27D may be coupled to the pixel electrode 31 via the opening 26b. The exemplary embodiment of FIG. 2C shows the drain electrode 27D coupled to the pixel electrode 31.

[0053] Referring to FIG. 2D, after forming the source and drain electrodes 27S and 27D, a passivation layer 28 may be formed on the entire surface of the insulating substrate. The passivation layer 28 may be formed by CVD or other like methods, and it may be made of SiO<sub>2</sub> or SiNx.

[0054] Next, an annealing process may be carried out to enhance the TFT's characteristics by curing damage arising during the fabrication process.

[0055] After annealing, a planarization layer 29 may be formed to remove a step of the lower structure. The pla-

narization layer 29 may be formed of acryl, polyimide (PI), polyamide (PA), benzocyclobutene (BCB), or other like materials.

[0056] Next, an opening 29a that exposes a portion of the pixel electrode 31 may be formed to define an emission region of the organic light emitting device OLED.

[0057] An organic layer 32 may then be formed on the entire surface of the insulating substrate 20 including the pixel electrode 31. The organic layer 32 may comprise several layers according to its function. Generally, in addition to an emission layer, the organic layer 32 may comprise a multi-layered structure including at least one of a hole injecting layer (HIL), a hole transporting layer (HTL), a hole blocking layer (HBL), an electron transporting layer (ETL), and an electron injecting layer (EIL).

[0058] The emission layer emits light having a specific wavelength when electrons and holes, which are injected from a cathode and an anode of the organic electroluminescence device OLED, recombine. At least one of an HIL, HTL, HBL, ETL, EIL, and the like, which have charge transporting capability, may be selectively inserted between an electrode and the emission layer to obtain highly efficient emission.

[0059] When the pixel electrode 31 of the organic electroluminescence device acts as an anode electrode, a subsequently formed upper electrode may act as a cathode electrode. In this case, an HIL and an HTL may be positioned between the pixel electrode 31 and the emission layer, and an HBL, an ETL and an EIL may be positioned between the emission layer and the subsequently formed upper electrode.

[0060] Further, when the pixel electrode 31 acts as a cathode electrode, the subsequently formed upper electrode may act as an anode electrode, resulting in an organic layer arrangement that may be opposite to the above-described arrangement.

[0061] Such an organic layer 32 including the emission layer may be formed by a wet coating method in which coating is performed in a solution state, such as spin coating, deep coating, spray, screen printing, inkjet printing, or other like methods, or by a dry coating method, such as sputtering, vacuum deposition, or other like methods.

[0062] After forming the organic layer 32, an upper electrode 33 may then be formed on the organic layer 32, thus forming the organic light emitting device OLED including the pixel electrode 31, the organic layer 32 and the upper electrode 33.

[0063] Although not shown in the drawings, an upper substrate may encapsulate the organic light emitting device OLED.

[0064] FIG. 3A, FIG. 3B and FIG. 3C are cross-sectional views showing a manufacturing process of an organic electroluminescence display according to a second exemplary embodiment of the present invention.

[0065] Referring to FIG. 3A, a transparent conductive material, such as ITO, IZO, or other like material, may be deposited and patterned on an insulating substrate 40 having a buffer layer 41 to form source and drain electrodes 42S and 42D and a pixel electrode 51.

[0066] Edge portions of the source and drain electrodes **42S** and **42D** and the pixel electrode **51** may have a taper angle of about 10° to about 45°.

[0067] Similar to the first embodiment, an active layer **43** of the TFT may then be formed by depositing an amorphous silicon layer, and forming and patterning a poly-Si layer through a crystallization process using a laser.

[0068] After the crystallization process, a portion of the poly-Si layer on the inclined edge portions of the source and drain electrodes **42S** and **42D** may have less crystallinity than a portion of the poly-Si layer that is not on the inclined edge portions of the source and drain electrodes **42S** and **42D**.

[0069] The active layer **43** may be unevenly formed due to the below source and drain electrodes **42S** and **42D**.

[0070] Referring to **FIG. 3B**, after forming the active layer **43**, a gate electrode **45** may be formed by depositing a gate insulating layer **44** on the active layer **43**, depositing a gate metal on the gate insulating layer **44**, and patterning the gate metal.

[0071] Next, source and drain regions **43S** and **43D** may be formed by doping impurity ions at a high concentration into the active layer **43** using the gate electrode **45** as a mask. A region between the source and drain regions **43S** and **43D** acts as the TFT's channel region **43C**.

[0072] Inclined portions of the source and drain regions **43S** and **43D** on the edge portions of the source and drain electrodes **42S** and **42D** become regions having a lower doping concentration, namely, LDD regions **43S-L** and **43D-L**, as compared to portions **43S-H** and **43D-H** of the source and drain regions **43S** and **43D** on other portions of the source and drain electrodes **42S** and **42D**. The portions **43S-H** and **43D-H** of the source and drain regions **43S** and **43D** on the source and drain electrodes **42S** and **42D** may act as highly doped regions **43S-H** and **43D-H**.

[0073] Referring to **FIG. 3C**, after forming the source and drain regions **43S** and **43D** having the LDD regions **43S-L** and **43D-L**, a passivation layer **46**, which may be made of SiO<sub>2</sub> or SiNx, may be formed on an entire surface of the insulating substrate **40** having the gate electrode **45**.

[0074] An annealing process may then be carried out in a furnace to further activate the impurities doped into the active layer **43** and enhance the TFT's characteristics by curing a damaged region arising in the TFT manufacturing process.

[0075] A planarization layer **47** may be formed on the entire surface of the insulating substrate **40** after performing the annealing process. Similar to the first exemplary embodiment, the planarization layer **47** may be made of acryl, polyimide (PI), polyamide (PA), benzocyclobutene (BCB), or other like materials.

[0076] An opening **47a** may then be formed to expose a portion of the pixel electrode **51** and define an emission region of the organic light emitting device OLED.

[0077] After forming the opening **47a**, an organic layer **52** may be formed on the pixel electrode **51**, similarly to the first exemplary embodiment.

[0078] Next, an upper electrode **53** may be formed on the organic layer **52**, thus forming the organic light emitting device OLED including the pixel electrode **51**, the organic layer **52**, and the upper electrode **53**.

[0079] Although not shown, an upper substrate may encapsulate the organic light emitting device OLED.

[0080] For the TFT formed as described above, the LDD region may be formed using one doping process and without a separate additional mask.

[0081] As described above, according to exemplary embodiments of the present invention, a TFT having an LDD structure and an organic electroluminescence display using the same may be achieved without adding a separate mask.

[0082] While the exemplary embodiments described above show an organic electroluminescence display, the present invention is not limited thereto and the TFT of the present invention may be utilized in any device using a TFT.

[0083] It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A thin film transistor (TFT), comprising:

a lightly doped drain (LDD) region formation pattern; and  
an active layer formed in an uneven structure on the LDD region formation pattern, and having a source region and a drain region including an LDD region.

2. The TFT of claim 1, wherein the LDD region formation pattern is formed of a transparent conductive material.

3. The TFT of claim 1, wherein the LDD region formation pattern has an edge portion with a taper angle of about 10° to about 45°.

4. The TFT of claim 1, wherein the LDD region is formed in an inclined region of the active layer on an edge portion of the LDD region formation pattern.

5. The TFT of claim 1, wherein the LDD region has less crystallinity than a remaining portion of the source region and the drain region.

6. The TFT of claim 1, further comprising:

a substrate; and

a buffer layer formed on the substrate,

wherein the LDD region formation pattern is formed on the buffer layer.

7. The TFT of claim 6, wherein the substrate is one of a glass substrate and a plastic substrate.

8. A display, comprising:

a lightly doped drain (LDD) region formation pattern and a pixel electrode formed on a same layer on a substrate;

an active layer formed in an uneven structure on the LDD region formation pattern, and having a source region and a drain region including an LDD region;

a gate electrode formed on a gate insulating layer; and

- a source electrode and a drain electrode coupled to the source region and the drain region, respectively,
- wherein either the source electrode or the drain electrode is coupled to the pixel electrode.
9. The display of claim 8, wherein the LDD region formation pattern is formed of a transparent conductive material.
10. The display of claim 8, wherein the LDD region formation pattern has an edge portion with a taper angle of about 10° to about 45°.
11. The display of claim 8, wherein the LDD region is formed in an inclined region of the active layer on an edge portion of the LDD region formation pattern.
12. The display of claim 8, wherein the LDD region has less crystallinity than a remaining portion of the source region and the drain region.
13. The display of claim 8, further comprising a buffer layer formed on the substrate.
14. The display of claim 8, further comprising:
- an insulating layer formed on an entire surface of the substrate having the source electrode and the drain electrode,
- wherein the insulating layer has an opening that defines an emission region by exposing a portion of the pixel electrode.
15. The display of claim 14, wherein the insulating layer comprises:
- a passivation layer formed of an inorganic material; and
- a planarization layer formed of an organic material.
16. The display of claim 15, wherein the passivation layer is a silicon dioxide (SiO<sub>2</sub>) layer or a silicon nitride (SiNx) layer.
17. The display of claim 15, wherein the planarization layer is formed of one of acryl, polyimide (PI), polyamide (PA), and benzocyclobutene (BCB).
18. A thin film transistor (TFT), comprising:
- a source electrode and a drain electrode formed on a substrate; and
- an active layer formed in an uneven structure on the source electrode and the drain electrode, and having a source region and a drain region including an LDD region.
19. The TFT of claim 18, wherein the source electrode and the drain electrode are formed of a transparent conductive material.
20. The TFT of claim 18, wherein the source electrode and the drain electrode have an edge portion with a taper angle of about 10° to about 45°.
21. The TFT of claim 18, wherein the LDD region is formed in an inclined region of the active layer on an edge portion of the source electrode and the drain electrode.
22. The TFT of claim 18, wherein the LDD region has less crystallinity than a remaining portion of the source region and the drain region.
23. The TFT of claim 18, further comprising a buffer layer formed on the substrate.
24. The TFT of claim 18, wherein the substrate is one of a glass substrate and a plastic substrate.
25. A display, comprising:
- a source electrode, a drain electrode, and a pixel electrode formed on a same layer on a substrate;
- an active layer having a source region and a drain region including an LDD region, and formed in an uneven structure on the source electrode and the drain electrode;
- a gate insulating layer formed on an entire surface of the substrate having the active layer;
- a gate electrode formed on the gate insulating layer;
- an insulating layer formed on an entire surface of the substrate having the gate electrode, and having an opening that defines an emission region by exposing a portion of the pixel electrode;
- an organic layer formed on the opening of the insulating layer; and
- an upper electrode formed on an entire surface of the substrate.
26. The display of claim 25, wherein either the source electrode or the drain electrode is integrally formed with the pixel electrode.
27. The display of claim 25, wherein the source electrode and the drain electrode are formed of a transparent conductive material.
28. The display of claim 25, wherein the source electrode and the drain electrode have an edge portion with a taper angle of about 10° to about 45°.
29. The display of claim 25, wherein the LDD region is formed in an inclined region of the active layer on an edge portion of the source electrode and the drain electrode.
30. The display of claim 25, wherein the LDD region has less crystallinity than a remaining portion of the source region and the drain region.
31. The display of claim 25, further comprising a buffer layer formed on the substrate.
32. The display of claim 25, wherein the insulating layer comprises:
- a passivation layer formed of an inorganic material; and
- a planarization layer formed of an organic material.
33. The display of claim 32, wherein the passivation layer is a silicon dioxide (SiO<sub>2</sub>) layer or a silicon nitride (SiNx) layer.
34. The display of claim 32, wherein the planarization layer is formed of one of acryl, polyimide (PI), polyamide (PA), and benzocyclobutene (BCB).
35. The display of claim 25, wherein the display is an organic electroluminescence display.
36. The display of claim 8, wherein the display is an organic electroluminescence display.

专利名称(译)	薄膜晶体管和使用其的有机电致发光显示器		
公开(公告)号	<a href="#">US20050242348A1</a>	公开(公告)日	2005-11-03
申请号	US11/095601	申请日	2005-04-01
[标]申请(专利权)人(译)	吴尚HUN		
申请(专利权)人(译)	吴尚HUN		
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摘要(译)

具有轻掺杂漏极 (LDD) 结构的薄膜晶体管 (TFT) 包括轻掺杂漏极 (LDD) 区域形成图案, 在LDD区域形成图案上的不平坦结构中形成的有源层, 并且具有源极区域和漏区具有LDD区。栅电极可以形成在栅极绝缘层上, 源电极和漏电极耦合到源区和漏区。

